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LCD Module Technical Specification

Final Revision

F-51854GNFJ-SLW-ABN

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Revision History

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1.General Specifications

Operating Temp. : min. -20°C ~max. 70°C

Storage Temp. : min. -20°C ~max. 70°C

Dot Pixels : 160 (W) × 128 (H) dots

Dot Size : $0.54 \text{ (W)} \times 0.54 \text{ (H)} \text{ mm}$

Dot Pitch : $0.58 \text{ (W)} \times 0.58 \text{ (H)} \text{ mm}$

Viewing Area : $108.6 \text{ (W)} \times 82.55 \text{ (H)} \text{ mm}$

Outline Dimensions : $129.0 (W) \times 102.0^* (H) \times 13.5 max. (D) mm$

* Without FPC

Weight : 160g max.

LCD Type : NSD-22808

(F-STN / Black &White-mode / Transflective)

Viewing Angle : 6:00

Data Transfer : 8-bit parallel data transfer

Serial data transfer

Backlight : LED Backlight / White

Additional Spec. : Winter White Display

(Highly Reflective Type Transflective Display)

Drawing : Dimensional Outline UE-211023

RoHS regulation : To our best knowledge, this product satisfies material

requirement of RoHS regulation.

Our company is doing the best efforts to obtain the equivalent certificate from our suppliers.

2.Electrical Specifications

2.1. Absolute Maximum Ratings

Vss=0V

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage	VDD-VSS	-	-0.3	6.0	V
(Logic)					
Supply Voltage	V3, Vоит	-	-0.3	+18.0	V
(LCD Drive)					
Supply Voltage	V1, V2, VC,	-	-0.3	V3	V
(LCD Drive)	MV1, MV2				
Input Voltage	Vin	-	-0.3	VDD+0.3	V
Output Voltage	Vouт	-	-0.3	Vpp+0.3	V

^{*1:}Voltages V₃, V₂, V₁, VC, MV₁, MV₂ and MV₃(Vss) must always meet the conditions of $V_3 \ge V_2 \ge V_1 \ge V_2 \ge MV_2 \ge MV_3 \ge MV_3 \le MV_3$

When inputting Vou⊤ from outside, maintain the condition of Vouт≥3+0.2V.

2.2.DC Characteristics

Ta=25°C, Vss=0V

						a-20 0, vo	
Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Supply Voltage	VDD-Vss	-		4.5	-	5.5	V
(Logic)							
Supply Voltage	Vouт	-		V _{DD2}	-	16.2	V
(LCD Drive)	Vз			5.6	-	16.2	
Supply Voltage	V _{DD2}	With Triple(Based on VDD)		4.5	-	5.3	٧
(Booster Circuit)							
Booster Output	Vouт	-		-	-	16.2	V
Voltage							
Voltage Regulator	Vз		*1	5.6	-	16.2	V
Operating Voltage							
"High" Level	Vih	VDD=4.5~5.5V		0.8×VDD	-	Vdd	V
Input Voltage			*2				
"Low" Level	VIL	VDD=4.5~5.5V		Vss	-	0.2×Vdd	V
Input Voltage			*2				
"High" Level	Vон	VDD=4.5~5.5V		0.8×VDD	-	Vdd	V
Output Voltage		Іон=-25µА *3					
"Low" Level	Vol	VDD=4.5~5.5V		Vss	-	0.2×Vdd	V
Output Voltage		loι=25μA *3					
Supply Current	loo	VDD-Vss=5.0V		-	1.2	1.8	mA
Oscillation	fcL			92	100	108	kHz
Frequency							

^{*1:} The V₃ voltage adjusting circuit is adjusted within the electronic volume operating range.

These ranges are applied when using the external power_supply.

^{*3:} D0~D7, FR, FRS, DOF and CL pins

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^{*2:}Voltage Vout must always meet the conditions of Vout≥Vdd.

^{*2:} A0, D0~D5, D6(SCL), D7(SI), RD(E), WR(R/W), CS1, CS2, CLS, CL, FR, M/S, C86, P/S, DOF, RES, IRS and HPM pins

2.3.AC Characteristics

2.3.1.Read/Write Operation Sequence (80 series CPU)

VDD=4.5~5.5V

VDD-4.3 (
Parameter		Symbol	Min.	Max.	Units	
Address Hold Time		t _{AH8}	0	-	ns	
Address Setup Time		t _{AW8}	0	-	ns	
System Write Cycle Time		t _{wcyc8}	500		ns	
System Read Cycle Time		t _{RCYC8}	7000	1	ns	
Control Low Pulse Width	WRITE	t _{CCLW}	200	ı	ns	
	READ	t _{CCLR}	3000	ı	ns	
Control High Pulse Width	WRITE	t cchw	200	1	ns	
	READ	t cchr	200	1	ns	
Data Setup Time		t _{DS8}	200	ı	ns	
Data Hold Time		t _{DH8}	30	ı	ns	
RD Access Time(CL=100pF)		t _{ACC8}		3500	ns	
Output Disable Time		t _{OH8}	5	200	ns	

^{*1:}This is in case of making the access by WR and RD, setting the CS=LOW.

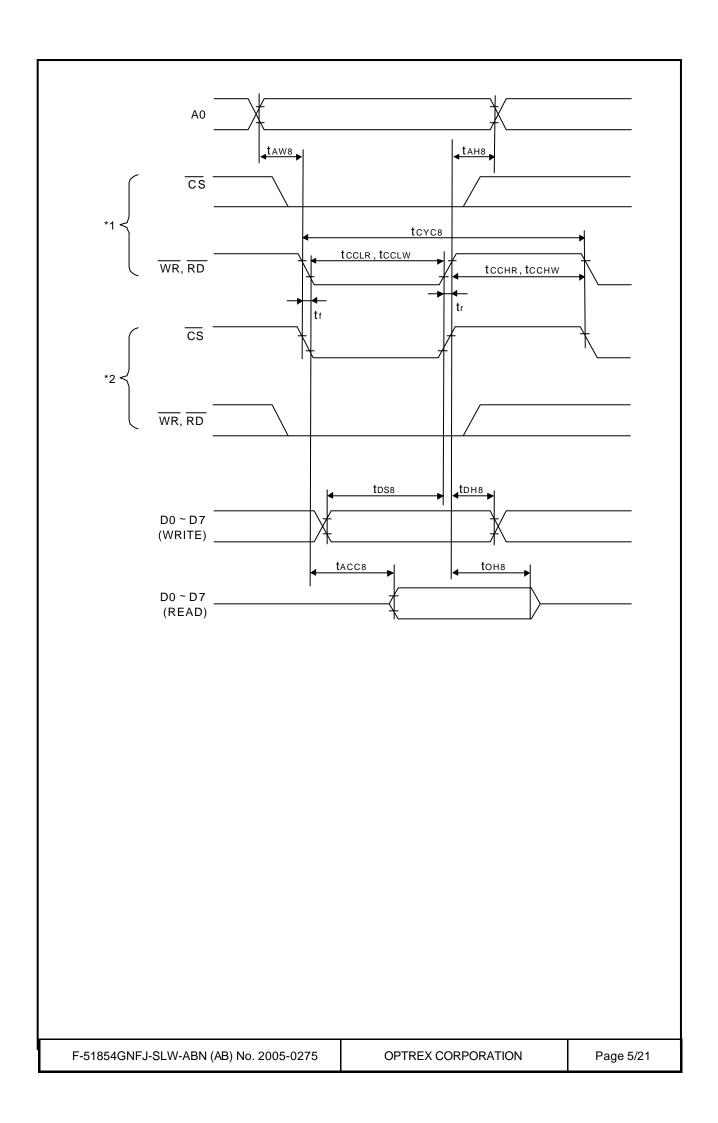
^{*2:}This is in case of making the access by $\overline{\text{CS}}$, setting the $\overline{\text{WR}}$, $\overline{\text{RD}}$ =LOW.

^{*3:} Input signal rise and fall time (tr, tf) must not exceed 15 ns.

When the system cycle time is used at a high speed, it is specified by (tr+tf)≤(tcγca-tcclw-tccнw) or (tr+tf)≤(tcγca-tcclr-tccнr).

^{*4:}Timing is entirely specified with reference to 20% or 80 % of VDD.

^{*5:}tcclw and tcclr are specified in terms of the overlapped period when CS is at LOW level and WR and RD are at LOW level.



2.3.2. Read/Write Operation Sequence (68 series CPU)

VDD=4.5~5.5V

Parameter	Symbol	Min.	Max.	Units	
Address Hold Time		t _{AH6}	20	-	ns
Address Setup Time		t _{AW6}	0	-	ns
System Write Cycle Time		t _{wcyc6}	500	-	ns
System Read Cycle Time		t _{RCYC6}	7000	-	ns
Enable High Pulse Width	READ	t _{EWHR}	3000	-	ns
	WRITE	t ewhw	200	-	ns
Enable Low Pulse Width	READ	t _{EWLR}	200	-	ns
	WRITE	t _{EWLW}	200	-	ns
Data Setup Time		t _{DS6}	200	-	ns
Data Hold Time		t _{DH6}	60	-	ns
Access Time (CL=100pF)		t _{ACC6}	-	3500	ns
Output Disable Time	·	t _{OH6}	5	200	ns

^{*1:}This is in case of making the access by E, setting the CS=LOW.

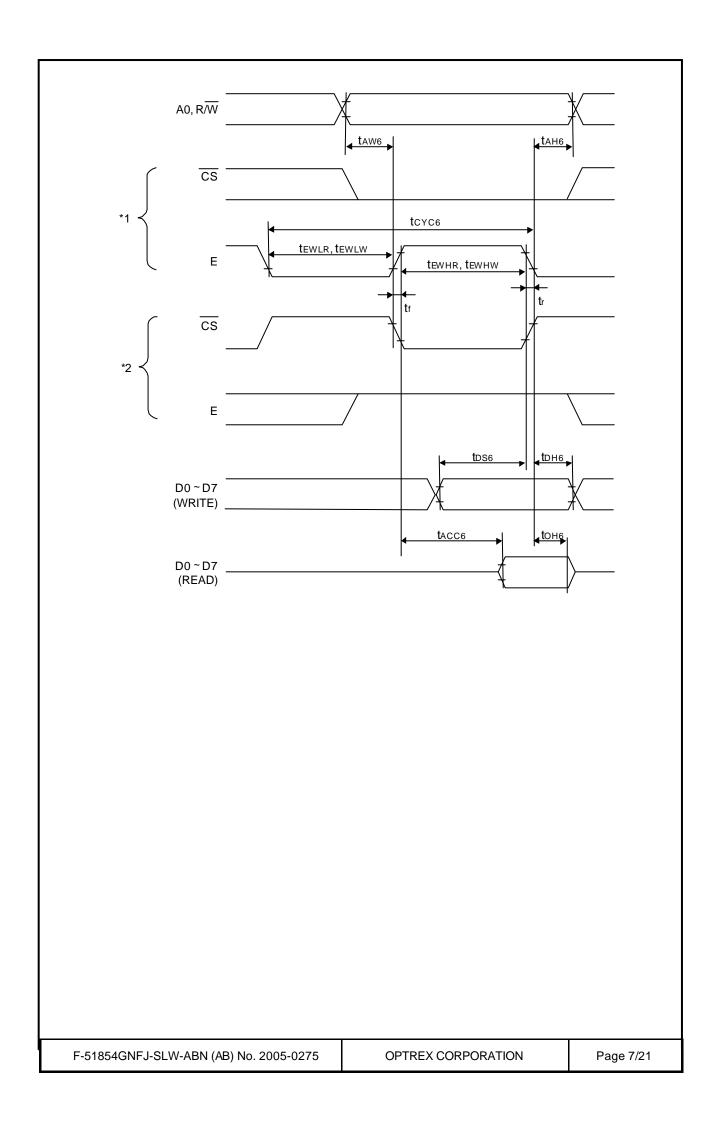
^{*2:}This is in case of making the access by $\overline{\text{CS}}$, setting the E=HIGH.

^{*3:} The rise time and the fall time (tr, tf) of the iput signal should be set to 15 ns or less.

When it is necessary to use the system cycle time at high speed, the rise time and the fall time should be so set to conform to (tr+tf)≤(tcyc6-tewlw-tewhw) or (tr+tf)≤(tcyc6-tewlr-tewhr).

 $^{^*4}$:All the timing should basically be set to 20% and 80 % of the V_{DD}.

^{*5:}tewLw , tewLR should be set to the overlapping zone where the \overline{CS} is on the LOW level and where the E is on the HIGH level.



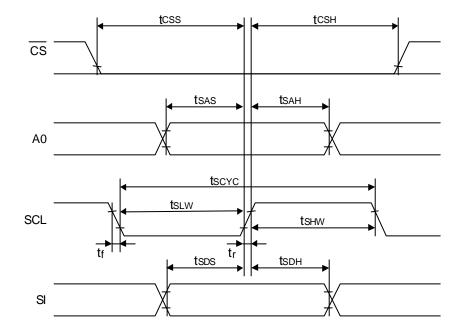
2.3.3. Serial Interface Sequence

VDD=4.5~5.5V

Parameter	Symbol	Min.	Max.	Units
Serial Clock Cycle	t _{scyc}	250	-	ns
SCL High Pulse Width	t _{SHW}	100	-	ns
SCL Low Pulse Width	t _{SLW}	100	-	ns
Address Setup Time	t _{SAS}	150	-	ns
Address Hold Time	t _{SAH}	150	-	ns
Data Setup Time	t _{sds}	200	-	ns
Data Hold Time	t _{SDH}	100	-	ns
CS-SCL Time	t _{css}	150	-	ns
CS-SCL Time	t _{CSH}	150	-	ns

^{*1:}Input signal rise and fall time (tr, tf) must not exceed 15ns.

 $^{^*2}$:Timing is entirely specified with reference to 20% or 80% of V_{DD} .



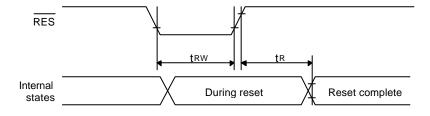
2.3.4. Display Control Timing Characteristics

Reset Input Timing

VDD=4.5~5.5V

Parameter	Symbol	Min.	Тур.	Max.	Units
Reset time	t _R	-	-	1000	
Reset "L" Pulse Width	\mathbf{t}_{RW}	1000	-	-	μs

^{*1:} Timing is entirely specified with reference to 20% or 80% of V_{DD} .



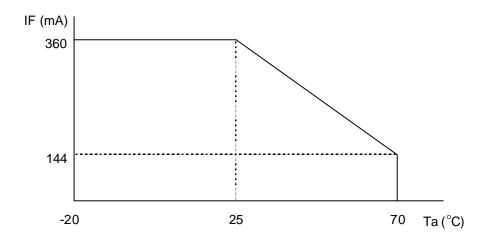
2.4. Lighting Specifications

2.4.1. Absolute Maximum Ratings

Ta=25°C

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Foward Current	l F	Note 1	ı	ı	360	mA
Reverse Voltage	VR	-	ı	1	5	V
LED Power Dissipation	PD	-	ı	-	1440	mW

Note 1 : Refer to the foward current derating curve.



2.4.2. Operating Characteristics

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Foward Voltage	VF	l=180mA	ı	3.5	4.0	V
Luminance of	L	l=180mA	28	40	-	cd/m ²
Module Surface						

3. Optical Specifications (MLA Driving)

3.1. Optical Characteristics

Ta=25°C, 1/65 Duty, 1/8 Bias, VoD=10.1V (Note 4), θ = 0°, ϕ =- °

Parameter		Symbol	Conditions	Min.	Тур.	Max.	Units
Contrast Ra	atio Note 1	CR	θ= 0°, φ=- °	-	5.0	ı	
Viewing Ang	gle		Shown in 3.2				
Response	Rise Note 2	Ton	-	-	125	200	ms
Time	Decay Note 3	Toff	-	-	200	300	ms

Note 1 :Contrast ratio is definded as follows.(CR = LOFF / LON)

LON: Luminance of the ON segments LOFF: Luminance of the OFF segments

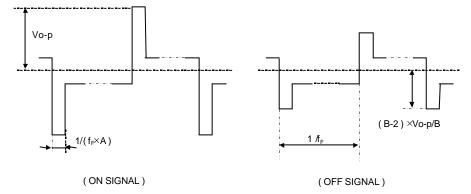
Measuring Spot: 3.0mm

- Note 2 :The time that the luminance level reaches 90% of the saturation level from 0% when ON signal is applied.
- Note 3 :The time that the luminance level reaches 10% of the saturation level from 100% when OFF signal is applied.
- Note 4: Definition of Driving Voltage Vod

Assuming that the typical driving waveforms shown below are applied to the LCD Panel at 1/A Duty - 1/B Bias (A: Duty Number, B: Bias Number). Driving voltage VoD is definded as follows.

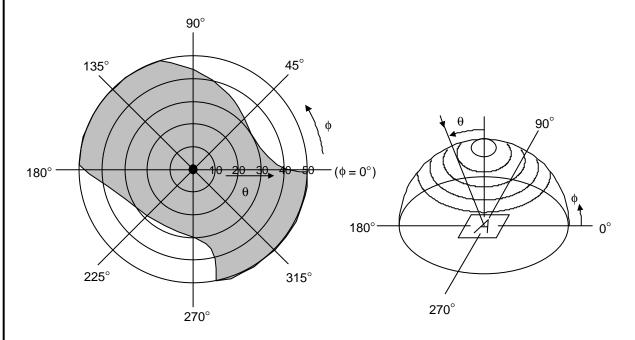
Vop = (Vth1+Vth2) / 2

- Vth1: The voltage Vo-P that should provide 70% of the saturation level in the luminance at the segment which the ON signal is applied to.
- Vth2: The voltage Vo-P that should provide 20% of the saturation level in the luminance at the segment which the OFF signal is applied to.



3.2. Definition of Viewing Angle and Optimum Viewing Area

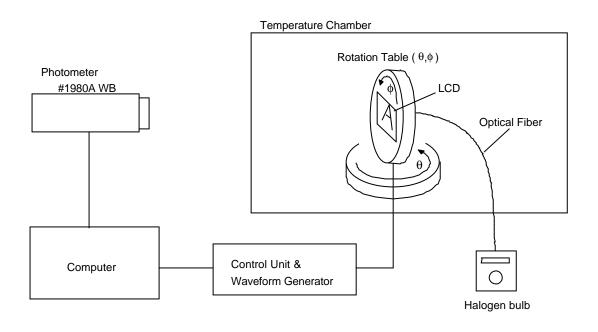
- *Point shows the point where contrast ratio is measured. : θ = 0°, ϕ =-°
- *Driving condition: 1/65 Duty, 1/8 Bias, VoD=10.1V, fF=72Hz



*Area shows typ. CR≥2.5(Measuring Spot : 3.0mm

ø)

3.3. System Block Diagram

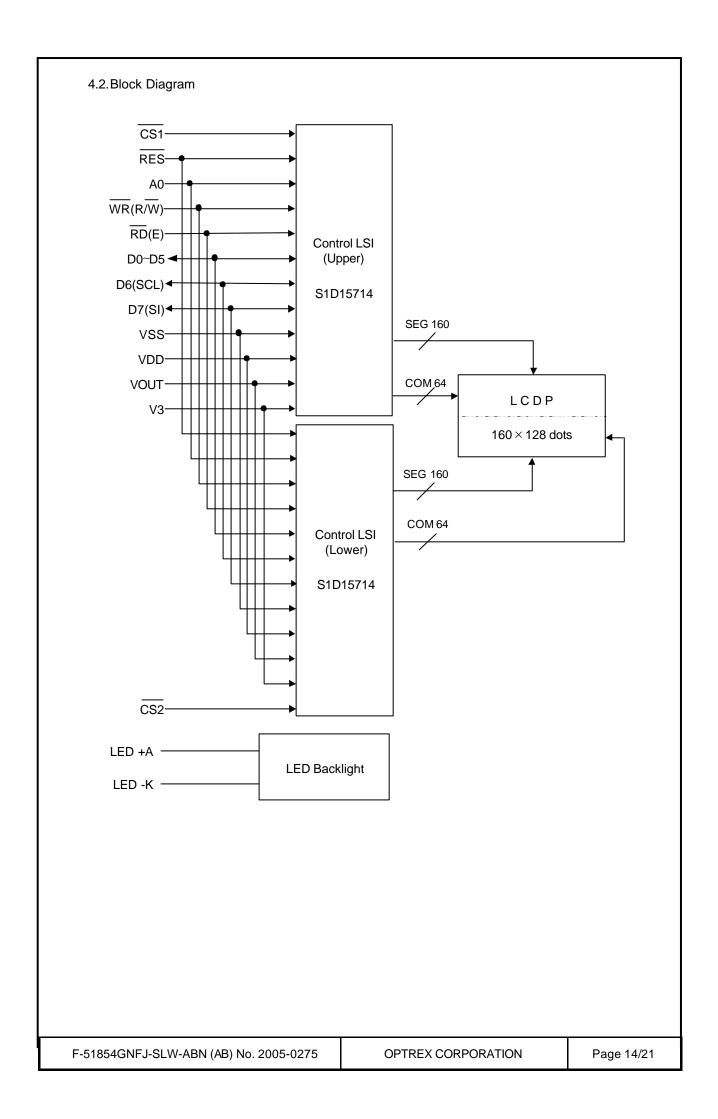


4.I/O Terminal

4.1. Pin Assignment

CN1

No.	Symbol	Function
1	CS1	Chip Select Signal L : Active (Upper Display)
2	CS2	Chip Select Signal L : Active (Lower Display)
3	RES	Reset Signal L : Reset
4	A0	H : D0~D7 are Display Data L : D0~D7 are Instructions
5	\overline{WR}	80 family CPU : Write Signal L : Active
	(R/W)	68 family CPU : Read/Write Select Signal H : Read
6	\overline{RD}	80 family CPU : Read Signal L : Active
	(E)	68 family CPU : Enable Signal H : Active
7	D0	Display Data
8	D1	Display Data
9	D2	Display Data
10	D3	Display Data
11	D4	Display Data
12	D5	Display Data
13	D6(SCL)	Display Data
14	D7(SI)	Display Data
15	Vss	Power Supply (0V, GND)
16	VDD	Power Supply for Logic
17	Vouт	DC/DC Voltage Converter Output
18	Vз	Power Supply for LCD Drive
19	LED +A	LED Anode Terminal
20	LED -K	LED Cathode Terminal



5.Test

No change on display and in operation under the following test condition.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.

Temperature: 20±5°C Humidity: 65±5%RH

tests will be not conducted under functioning state.

No.	Parameter	Conditions	Notes
1	High Temperature Operating	70°C±2°C, 96hrs (operation state)	
2	Low Temperature Operating	-20°C±2°C, 96hrs (operation state)	1
3	High Temperature Storage	70°C±2°C, 96hrs	2
4	Low Temperature Storage	-20°C±2°C, 96hrs	1,2
5	Damp Proof Test	40°C±2°C,90~95%RH, 96hrs	1,2
6	Vibration Test	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz	3
		One cycle 60 seconds to 3 directions of X, Y, Z for each 15 minutes	
7	Shock Test	To be measured after dropping from 60cm high on the concrete surface in packing state. Dropping method comer dropping A corner: once Edge dropping B,C,D edge: once Face dropping E,F,G face: once	

Note 1: No dew condensation to be observed.

Note 2 :The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after removed from the test chamber.

Note 3: Vibration test will be conducted to the product itself without putting it in a container.

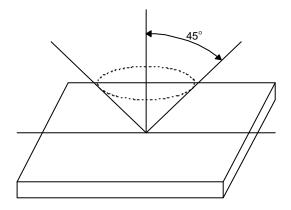
6. Appearance Standards

6.1. Inspection conditions

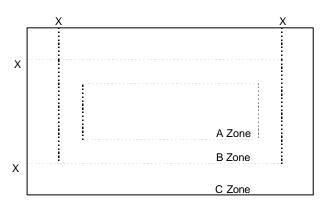
The LCD shall be inspected under 40W white fluorescent light.

The distance between the eyes and the sample shall be more than 30cm.

All directions for inspecting the sample should be within 45° against perpendicular line.



6.2. Definition of applicable Zones



X : Maximum Seal Line

A Zone: Active display area

B Zone : Out of active display area ~ Maximum seal line

C Zone : Rest parts

A Zone + B Zone = Validity viewing area

6.3. Standards (middle scale, LED)

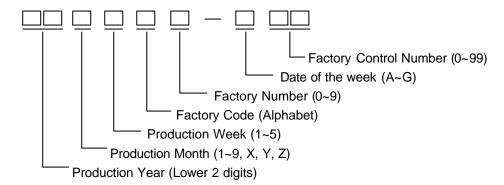
D = (Long + Short) / 2 *: Disregard Units: mm

No.	Parameter			Crite	ria
1	The Shape of Dot	(1) Pin Hole			
		\ <u>\</u>	Dimensio	n	Acceptable Number
			D ≤ 0	.10	*
			0.10 < D ≤ 0.	20	1 pc / dot(only segment)or less 5 pcs / cell or less
		(2) Breakage o	or Chips / Defor	mation	
		1.0	Oot Type		
			Dimension		Acceptable Number
		A →	A≤0.10		*
				(Shou	lld not be connected to next dot)
				1 pc /	dot(only segment)or less
		□ → R	0.10 <a≤0.15< td=""><td>5 pcs</td><td>/ cell or less</td></a≤0.15<>	5 pcs	/ cell or less
		J		(Shou	ld not be connected to next dot)
			B ≤ 0.15		*
		2.0	Defective type e	extends	over multiple numbers of dots
		\downarrow	Dimension		Acceptable Number
			D≤0.10		*
				1 pc /	dot(only segment)or less
			0.10 <d≤0.20< td=""><td>5 pcs</td><td>/ cell or less</td></d≤0.20<>	5 pcs	/ cell or less
			0.10×D±0.20	(Individ	dual dot must secure 1/2 area
				or mo	ore)
					_

No.	Parameter		C	Criteria		
2	Black and	(1) Round Sha	pe			
	White Spots,	Zone		Acceptable Number		
	Foreign Substances	Dimension		Α	В	С
		D ≤ 0.10		*	*	*
		0.10<	D ≤ 0.20	6	6	*
		0.20< D ≤ 0.30		4	4	*
		Individual dot must secure 1/2 area or more. (2) Line Shape				
		(_)	Zone	Acc	eptable Numb	er
		Length	Width	A	В	С
		*	W≤0.03	*	*	*
		L ≤2.0	0.03 <w≤0.05< td=""><td>5</td><td>5</td><td>*</td></w≤0.05<>	5	5	*
		L ≤1.0	≤0.10	4	4	*
		*	0.10 <w< td=""><td>In the san</td><td>ne way (1)</td><td>*</td></w<>	In the san	ne way (1)	*
		·	n 9pcs as total.	ıbstance Dei	fects")	
3 4	Color Variation Air Bubbles (between glass & polarizer)	·	•		eptable Numb	per C
	Air Bubbles (between glass	Not to be cons	spicuous defects. Zone	Acc A	eptable Numb	С
	Air Bubbles (between glass	Not to be cons Dimension 0.30<	spicuous defects. Zone $D \leq 0.30$	Acc A *	eptable Numb B	C *
	Air Bubbles (between glass	Dimension 0.30< 0.40< No more tha	spicuous defects. Zone $D \le 0.30$ $D \le 0.40$	Acc A * 3 2	eptable Numb B * *	C *
	Air Bubbles (between glass	Dimension 0.30< 0.40< No more that (Refer to "Co	pmplex Foreign Subspicuous defects. Zone $D \le 0.30$ $D \le 0.40$ $D \le 0.60$ n 3pcs as total.	Acc A * 3 2	eptable Numb B * *	C *
4	Air Bubbles (between glass & polarizer)	Dimension 0.30< 0.40< No more that (Refer to "Co	spicuous defects. Zone $D \le 0.30$ $D \le 0.40$ $D \le 0.60$	Acc A * 3 2	eptable Numb B * 3 fects")	* *
5	Air Bubbles (between glass & polarizer) Polarizer Scratches	Dimension 0.30< 0.40< No more that (Refer to "Co" Not to be constituted in the stains are not defective.	spicuous defects. Zone $D \le 0.30$ $D \le 0.40$ $D \le 0.60$ In 3pcs as total. Simplex Foreign Subspicuous defects.	Acc A * 3 2 substance Def	eptable Numb B * 3 fects")	C * * module is
5 6	Air Bubbles (between glass & polarizer) Polarizer Scratches Polarizer Dirts	Dimension 0.30< 0.40< No more that (Refer to "Co" Not to be considered in the stains are not defective. Black spots, line	spicuous defects. Zone $D \le 0.30$ $D \le 0.40$ $D \le 0.60$ In 3pcs as total. Implex Foreign Subspicuous defects. Expicuous defects. The removed easily approximately spicuous defects.	Acc A * 3 2 ubstance Def	eptable Numb B * * 3 fects")	C * * module is

7.Code System of Production Lot

The production lot of module is specified as follows.



8.Type Number

The type number of module is specified as follows.

F-51854GNFJ-SLW-ABN

9. Applying Precautions

Please contact us when questions and/or new problems not specified in this Specifications arise.

10.Precautions Relating Product Handling

The Following precautions will guide you in handling our product correctly.

- 1) Liquid crystal display devices
 - 1. The liquid crystal display device panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
 - 2. The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.
- 2) Care of the liquid crystal display module against static electricity discharge.
 - 1. When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti static mats (made of rubber), to protect work tables against the hazards of electrical shock.
 - 2. Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
 - 3. Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.
- 3) When the LCD module alone must be stored for long periods of time:
 - 1. Protect the modules from high temperature and humidity.
 - 2. Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
 - 3. Protect the modules from excessive external forces.
- 4) Use the module with a power supply that is equipped with an overcurrent protector circuit, since the module is not provided with this protective feature.
- 5) Do not ingest the LCD fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LCD fluid, wash immediately with soap.
- 6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.
- 7) For models which use CFL:
 - 1. High voltage of 1000V or greater is applied to the CFL cable connector area. Care should be taken not to touch connection areas to avoid burns.
 - 2. Protect CFL cables from rubbing against the unit and thus causing the wire jacket to become worn.
 - 3. The use of CFLs for extended periods of time at low temperatures will significantly shorten their service life.
- 8) For models which use touch panels:
 - 1. Do not stack up modules since they can be damaged by components on neighboring modules.
 - 2. Do not place heavy objects on top of the product. This could cause glass breakage.
- 9) For models which use COG, TAB, or COF:
 - 1. The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
 - 2. Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage, avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.

- 10) Models which use flexible cable, heat seal, or TAB:
 - 1. In order to maintain reliability, do not touch or hold by the connector area.
 - 2. Avoid any bending, pulling, or other excessive force, which can result in broken connections.
- 11)In case of buffer material such as cushion / gasket is assembled into LCD module, it may have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC, etc.,) depending on its materials.

Please check and evaluate these materials carefully before use.

12) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film..

Please check and evaluate those acrylic materials carefully before use.

11.Warranty

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- 2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
- 4. When the product is in CFL models, CFL service life and brightness will vary According to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- 5. We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.
- 6. Optrex will not be held responsible for any quality guarantee issue for defect products judged as Optrex-origin longer than 2 (two) years from Optrex production or 1(one) year from Optrex, Optrex America, Optrex Europe delivery which ever comes later.